規格書
DataSheet

CUSTOMER :

Company Name

Allied Vision

Model NO :

FW-PCIE02

DESCRIPTION :

OHCI 1.1 Compliant IEEE 1394a to PCI Express Host Adapter

Revision :

1.0

CUSTOMER APPROVED	APPROVAL	ENGINNER	ISSUE BY

IOI Technology Corporation
映奧股份有限公司
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- **Integrated Circuit**

Datasheet of XIO2200A
More Information on Website: http://www.ti.com/

Certifications :

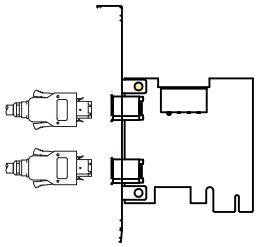
- **CE**
- **FCC**

RoHS Statement :

FW-PCIE02 Overview

Introduction:

The FW-PCIE02 is a 2-port OHCI 1.1 Compliant IEEE 1394a to PCI Express Host Adapter featuring Texas Instruments XIO2200A controller.



Highlight :

- Two external FireWire ports (support FireWire plug with latch type cable)
- Low-profile PCI form factor
- Provide big IDE power connector for supplying 1394 bus power.

Specification:

PCI Express:	- Supports 1-lane 2.5 Gb/s PCI Express. - Utilizes 100-MHz Differential PCI Express Common Reference Clock - Fully Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 - Fully Compliant with PCI Express Base Specification, Revision 1.0a - Fully Compliant with PCI Local Bus Specification, Revision 2.3 - A Second Virtual Channel for Quality-of-Service and Isochronous Applications - Advanced PCI Isochronous Windows for Memory Space Mapping to a Specified Traffic Class
IEEE 1394 Std Support:	- Fully compliant with provisions of IEEE Std 1394-1995 for high-performance serial bus and the IEEE Std 1394a-2000. - Fully Compliant with 1394 Open Host Controller Interface Specification, Revision 1.1. - Full IEEE Std 1394a?2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-by Concatenation, and Port Disable/Suspend/Resume. - Two IEEE Std 1394a-2000 Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, and 400M Bits/s. - EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric.
Power Management:	- Support for D1, D2, D3hot, and D3cold - Active State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States. - Wake Event and Beacon Support
FireWire ports:	Two External FW-6pin

RoHS:

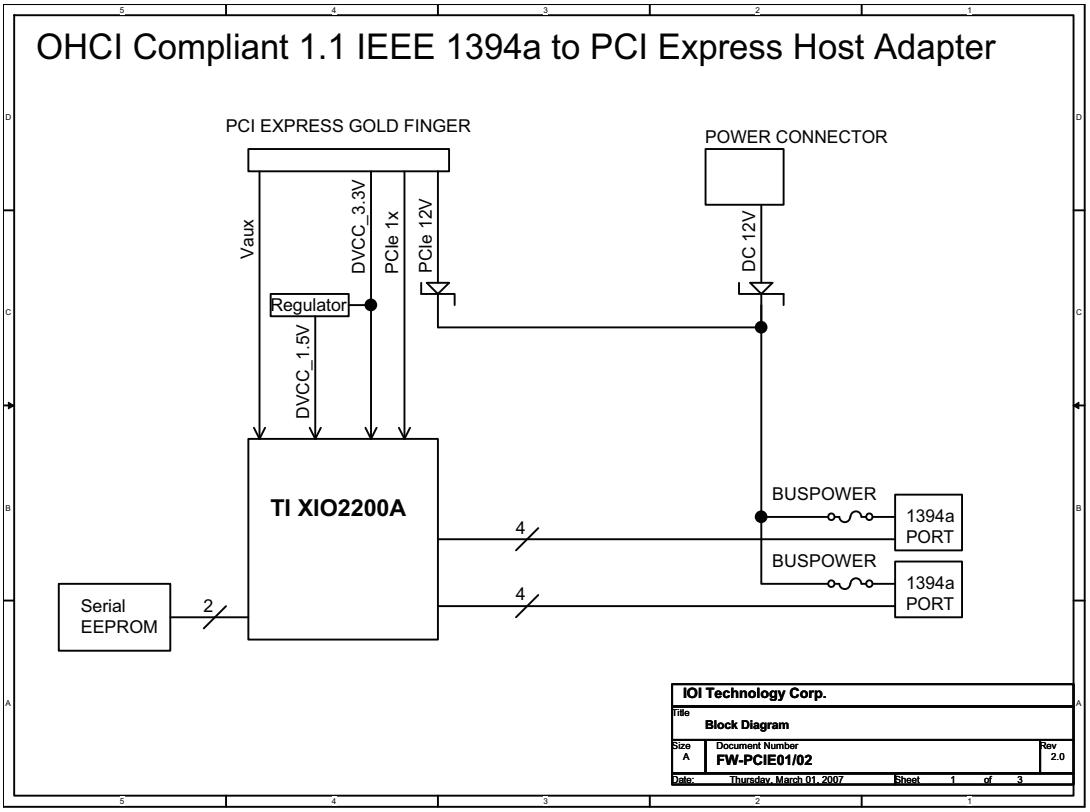
This Host Adapter is satisfied with RoHS regulations. Material of solder is satisfied with following definition.

	Material of solder
Solder Paste	SN-3.0AG-0.5CU
Flow and hand soldering	SN-0.7CU+NI

Environmental Condition:

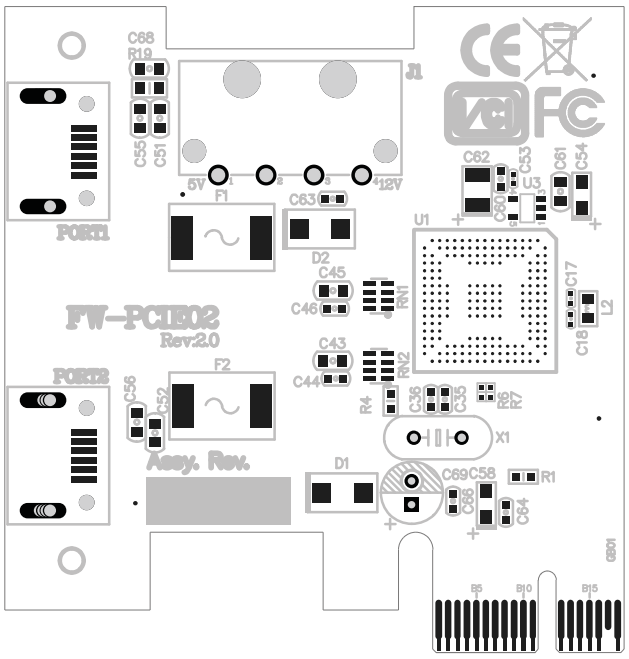
Operating free-air temperature: 0 ~ 65 degree C
Storage temperature range: -20 ~ 100 degree C
Humidity Operating : 0 ~ 80% RH, Non-condensing

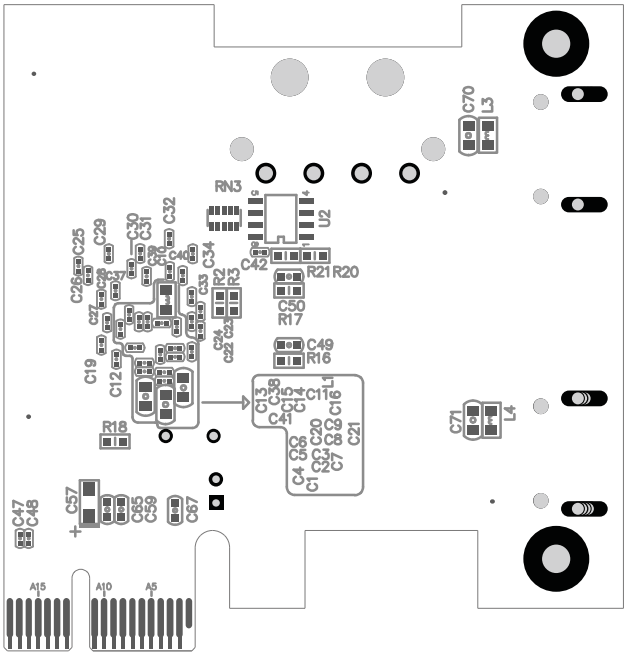
Block Diagram :



Silk Screen and Pictures

Silk Screen of FW-PCIE02 P.C.B. :

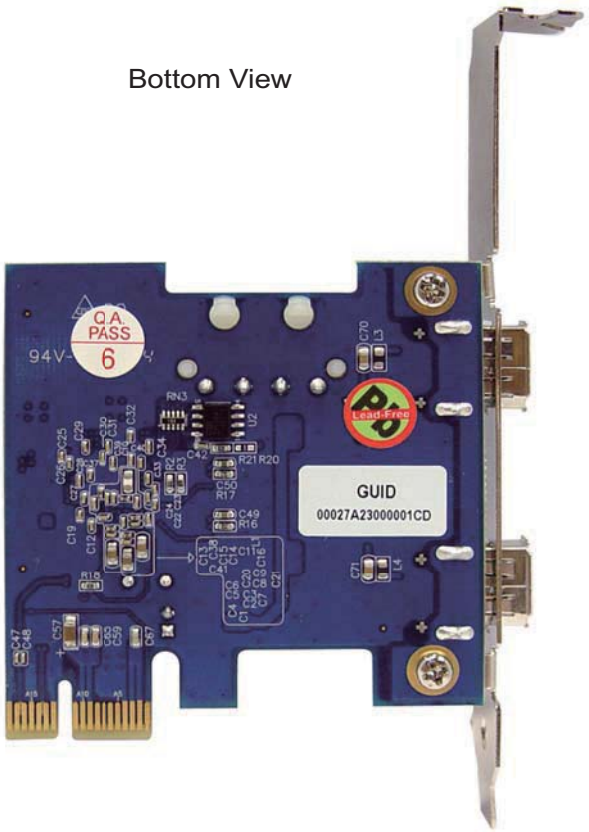




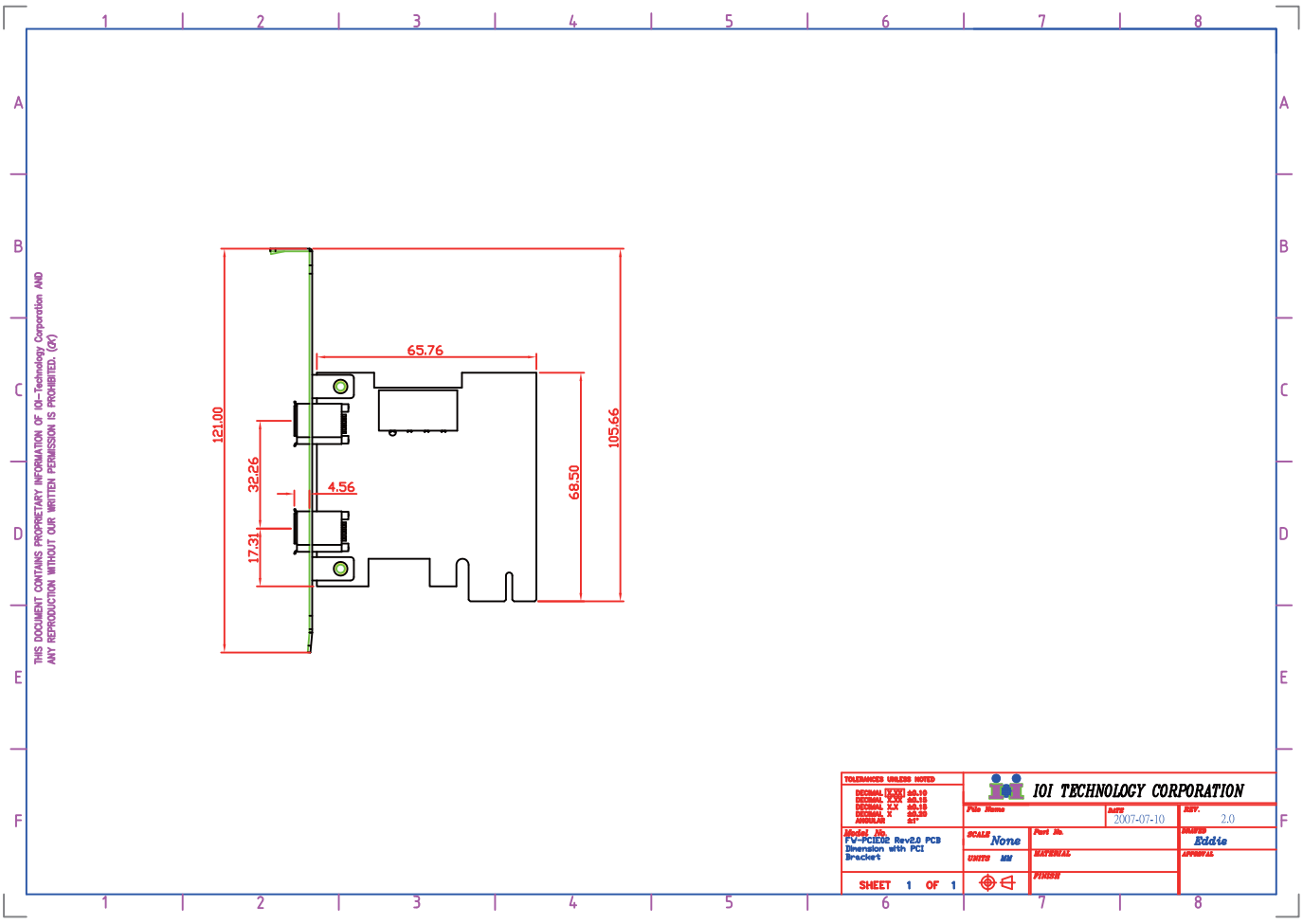
Picture of FW-PCIE02 PCBA:

Top View

Bottom View

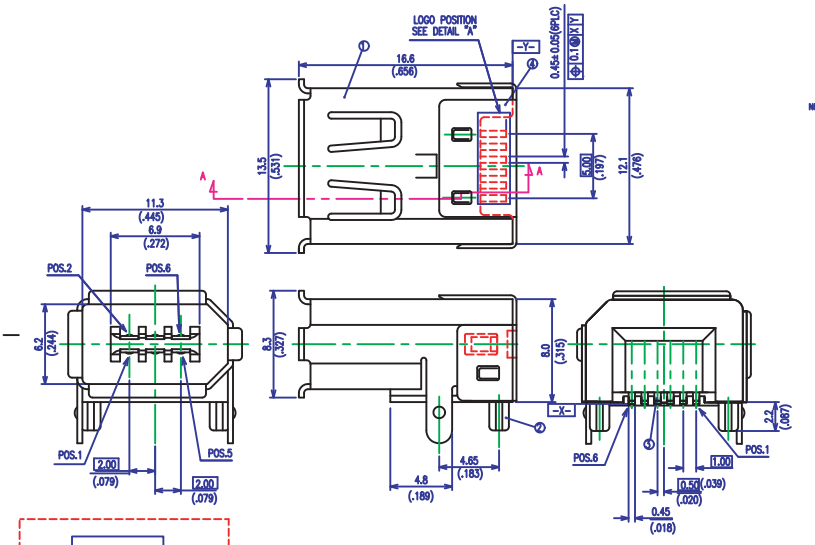


Mechanical Dimension



Datasheet of FireWire Connector

REV	DATE	REMARK



NOTES: UNLESS OTHERWISE SPECIFIED:

1.0 CONNECTOR ELECTRICAL CHARACTERISTICS:
1.1 WITHSTANDING VOLTAGE: DC 500 ± 50 V
1.2 INSULATION RESISTANCE: 100 MEGOHMS Min.
1.3 CONTACT RESISTANCE: 30 MILLIOHMS Max.
2.0 MATERIALS:
2.1 HOUSING: HIGH TEMPERATURE THERMOPLASTICS, UL94V-0.
2.2 SHELL: COPPER ALLOY
2.3 CONTACTS: COPPER ALLOY
2.4 BACK SHELL: STEEL
3.0 FINISH:
3.1 SHELL: TIN-LEAD OR BRIGHT TIN-LEAD PLATING OR BRIGHT TIN PLATING AND NI
3.2 CONTACTS: PLATED GOLD IN MATING AREA; Sn-Cu ON TAILS.
4.0 OTHERS:
4.1 ALL DIMENSIONS ARE IN MILLIMETERS WITH INCH EQUIVALENTS SHOWN IN BRACKETS.
4.2 DIMENSIONING PER ANSI Y14.5M-1982.
4.3 THE DRAWING ARE REDREW.

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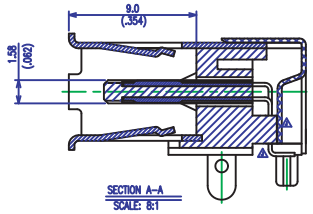
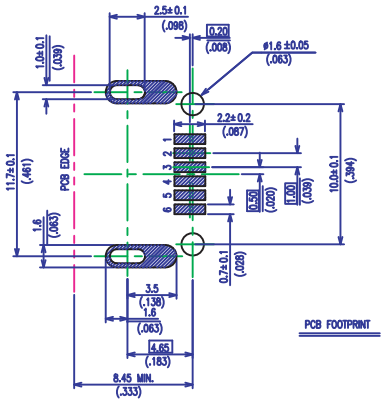
DECIMAL X.XX ±0.10	IOI TECHNOLOGY CORPORATION			
DECIMAL X.XX ±0.15	File Name CO-M0015	Date	Rev 1.0	
DECIMAL X.X ±0.15	Model No. CO-M0015	Scale NONE	Part No. CO-M0015	Drawed V-0562
DECIMAL X ±0.20		Units m m	Material NONE	Approval
ANGULAR ±1°	Sheet 1 of 2		Finish NONE	A4

REV	DATE	REMARK





PRODUCT NUMBERING CODE:

FWR41 – 6 X X X 0 X
1 2 3 4 5 6

1. CONNECTOR STYLE:
FWR41: IEEE 1394 (FIREWIRE) CONNECTOR, RIGHT ANGLE, RECEPTACLE, B/M (BOARD-MOUNT),FLAT,SMT TYPE, WITH BACKSHELL, h=4.50mm (h=CENER OF MATING FACE TO PCB)
2. NO. OF CONTACTS:
6: 6 POSITIONS.
3. COLOR OF HOUSING.
N: NATURAL COLOR.
K: BLACK COLOR.
G: PANTONE 424C
4. PLATING THICKNESS IN CONTACT MATING AREA:
5: 30u" GOLD IN MATING AREA; Sn-Cu ON TAILS.
2 : 5u" GOLD PLATING
8 : 30u" Au CONTACT AREA MATT Sn TERMINATION AREA
5. PLATING OF SHELL AND MARK CHANGES: SEE TABLE A
6. PACKAGING OF PRODUCTS
0 : TRAY
1 : TAPE & REEL

TABLE A:

CODE	DESCRIPTION
1	TIN-LEAD PLATING, W/O LOGO
3	SEE DRAWING NO. C-FWR41-01-00
4	TIN-LEAD PLATING, ACON LOGO
5	BRIGHT TIN-LEAD PLATING, W/O LOGO
C	BRIGHT TIN PLATING, W/O LOGO
G	BRIGHT TIN PLATING, WITH ACON LOGO
J	NI PLATING, W/O LOGO
T	NI PLATING, WITH ACON LOGO
H	SEE DRAWING NO. C-FWR41-02-00

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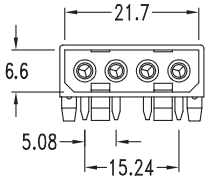
DECIMAL X.XX ±0.15	File Name CO-M0015	Date	Rev 1.0	
DECIMAL X.X ±0.15	Model No. CO-M0015	Scale NONE	Part No. CO-M0015	Drawed V-0562
DECIMAL X ±0.20		Units m m	Material NONE	Approval
ANGULAR ±1°	Sheet 2 of 2		Finish NONE	A4

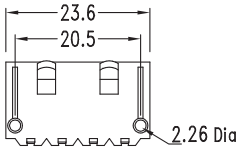
Datasheet of Wafer Connector

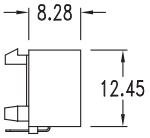
REV	DATE	REMARK

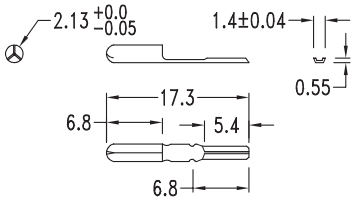
Features/Specifications:

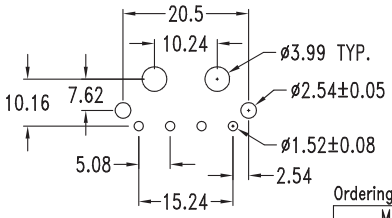
- UL 94V-2 nylon 66, Natural color
- Pins: Phosphor bronze Thickness 0.25mm
- Plating tin
- Two P.C tail lengths
- Voltage Rating: 250V AC (R.M.S)
- Current Rating: 6.5 amperes
- Dielectric Withstanding Voltage: 1500 VAC for 60 sec.
- Insulation Resistance: 500 megohms milliohms
- Contact Resistance: 10 milliohms maximun
- Ambient Temperature Range: -40°C to 105°C

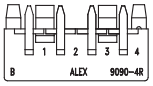












Ordering Information

Model No.	P.C Tail Lengtb
CO-M0019	3.6±0.5mm

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DECIMAL .XXX ±0.15
DECIMAL X.X ±0.15
DECIMAL X ±0.20
ANGULAR ±1°

IOI TECHNOLOGY CORPORATION

File Name: CO-M0019		Date:	Rev: 1.0
Model No.: CO-M0019	Scale: NONE	Part No.: CO-M0019	Drawed: V-0431
	Units: m m	Material: NONE	Approval:
Sheet 1 of 1		Finish: NONE	A4

1 XIO2200A Features

- Full x1 PCI Express Throughput
- Fully Compliant with *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- Fully Compliant with *PCI Express Base Specification*, Revision 1.0a
- Fully Compliant with *PCI Local Bus Specification*, Revision 2.3
- A Second Virtual Channel for Quality-of-Service and Isochronous Applications
- Advanced PCI Isochronous Windows for Memory Space Mapping to a Specified Traffic Class
- Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock
- Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000.
- Fully Compliant with *1394 Open Host Controller Interface Specification*, Revision 1.1
- Full IEEE Std 1394a−2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-by Concatenation, and Port Disable/Suspend/Resume
- Two IEEE Std 1394a-2000 Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, and 400M Bits/s
- Cable Ports Monitor Line Conditions for Active Connection To Remote Node
- Cable Power Presence Monitoring
- EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric
- Wake Event and Beacon Support
- Support for D1, D2, $D3_{hot}$, and $D3_{cold}$
- Active State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States
- Integrated AUX Power Switch Drains V_{AUX} Power Only When Main Power Is Off
- Eight 3.3-V, Multifunction, General-Purpose I/O Terminals
- Compact Footprint, 176-Ball, GGW MicroStar™ BGA, Lead-Free 176-Ball, ZGW MicroStar™ BGA, or Lead−Free 175−ball, ZHH MicroStar™ BGA

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2 Introduction

The Texas Instruments XIO2200A is a single-function PCI Express to PCI local bus translation bridge where the PCI bus interface is internally connected to a 1394a-2000 open host controller link-layer controller with a two-port 1394a PHY. When the XIO2200A is properly configured, this solution provides full PCI Express and 1394a functionality and performance.

2.1 Description

The XIO2200A is a single-function PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394a open host controller link-layer controller with a two-port 1394a PHY. The PCI-Express to PCI translation bridge is fully compatible with the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394a OHCI controller function is fully compatible with IEEE Standard 1394a-2000 and the latest 1394 *Open Host Controller Interface (OHCI) Specification*.

For downstream traffic, the PCI Express to PCI translation bridge simultaneously supports up to eight posted and four nonposted transactions for each enabled virtual channel (VC). For upstream traffic, up to six posted and four nonposted transactions are simultaneously supported for each VC.

The PCI Express interface supports a x1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Two independent VCs are supported. The second VC is optimized for isochronous traffic types and quality-of-service (QoS) applications. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the *PCI Express Base Specification*, Revision 1.0a. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency across the bridge. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The bridge provides physical write posting and a highly tuned physical data path for SBP-2 performance. The bridge is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, and 400M bits/s. The bridge provides two 1394 ports that have separate cable bias (TPBIAS). The bridge also supports the IEEE Std 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCI Express, and it provides plug-and-play (PnP) compatibility.

The PHY-layer provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

Power management (PM) features include active state link PM, PME mechanisms, the beacon and wake protocols, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported.

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCI Express configuration space, allow for further system control and customization.