CUSTOMER : 
Company Name

Allied Vision

Model NO :
FWB-PCIE1X11

DESCRIPTION :
Three ports FireWire 800 (IEEE-1394b) to PCI Express Host Adapter

Revision :
1.1.2

CUSTOMER APPROVED

APPROVAL

ENGINEER

ISSUE BY

IOI Technology Corporation
映奧股份有限公司
台北縣新店市寶橋路235巷125號4樓
4F, No.125, Lane 235, Pao Chiao Road,
Hsin Tian City, Taipei, Taiwan, R.O.C.
TEL : 02-89191358  FAX : 02-89191359
Introduction:

FWB-PCIE1X11 is designed with Texas Instruments XIO2213 B controller. The Texas Instruments XIO2213 B is a PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394b open host controller link-layer controller with a three-port 1394b PHY. The PCI-Express to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Standard 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s.

FWB-PCIE1X11 provides full PCI Express and 1394b functionality and performance.

<table>
<thead>
<tr>
<th>Specification:</th>
<th></th>
</tr>
</thead>
</table>
| PCI Express:            | • Full x1 PCI Express Throughput
                          • Fully Compliant with PCI Express Base Specification, Revision 1.1
                          • Utilizes 100-MHz Differential PCI Express Common Reference Clock |
| OHCI (Open Host Controller Interface): | • Fully supports provisions of IEEE P1394b-2002
                              • Fully Compliant with 1394 Open Host Controller Interface Specification, Revision 1.1 and Revision 1.2 draft
                              • Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, 400M Bits/s, and 800M Bits/s
                              • Cable Ports Monitor Line Conditions for Active Connection To Remote Node
                              • Cable Power Presence Monitoring
                              • EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric
                              • Active State Link Power Management Saves Power When Packet Activity on the PCI Express™ Link is Idle, Using Both L0s and L1 States
                              • Support for D1, D2, D3hot |
| Number of Ports:        | **FWB-PCIE1X11A:**
                          Two Bilingual IEEE Std 1394b-2002 Cable Ports
                          One FireWire IEEE Std 1394a-2000 Cable Port
                          **FWB-PCIE1X11B:**
                          Three Bilingual IEEE Std 1394b-2002 Cable Ports |
| Bus Power Connector:    | Big IDE 4-pin DC Power Connector |
Operating System Requirements:
The 1394b function (host driver) is supported (built in) by the following OS:
- Windows 2000 SP4 or later
- Windows XP SP2 or later
- Windows Vista SP1 or later
- Windows 8 and 8.1
- Mac OS 10.4 or later
- Linux kernel 2.6.23 or later.

RoHS:
This Host Adapter is satisfied with RoHS regulations. Material of solder is satisfied with following definition.

<table>
<thead>
<tr>
<th>Material of solder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Paste</td>
</tr>
<tr>
<td>SN-3.0AG-0.5CU</td>
</tr>
<tr>
<td>Flow and hand soldering</td>
</tr>
<tr>
<td>SN-0.7CU+NI</td>
</tr>
</tbody>
</table>

Environmental Condition:
Operating free-air temperature: 0 ~ 65 degree C
Storage temperature range: -20 ~ 100 degree C
Humidity Operating: 0 ~ 80% RH, Non-condensing

Block Diagram:

FireWire 800 (1394b) to PCI Express Host Adapter
Silk Screen and Pictures

Silk Screen of FWB-PCIE1x11 P.C.B.:

Picture of FWB-PCIE1x11:

FWB-PCIE1X11A

FWB-PCIE1X11B
Datasheet of Bilingual Connector

NOTES:
1) MATERIAL:
HOUSING: Thermoplastic, UL94V-0
CONTACT: Copper Alloy
SHELL: BRASS
2) PLATING:
Please refer to order information

TOLERANCES UNLESS NOTED

<table>
<thead>
<tr>
<th>Model No.</th>
<th>Scale</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>05-0101</td>
<td>NONE</td>
<td>G05-0101</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Electrical Specifications:
   Voltage: 30V
   Current: 1.5 Amps
   Contact Resistance: 50mΩ max.
   Shell Resistance: 50mΩ
   Insulation Resistance: 100 MΩ min.
   Dielectric Withstand: 100Vdc
2. Temperature Range:
   Operating: -40°C ~ +85°C
   Storage: -40°C ~ +105°C
   The Clearance between the contact and PCB no more than 0.10mm

View of Coplanarity

Coplanarity of solder pins=0.10mm total
## Datasheet of non-linear Thermistor

### Tolerances Table

<table>
<thead>
<tr>
<th>Tolerance</th>
<th>Decimal</th>
<th>Angular</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>±0.20</td>
<td>±1°</td>
</tr>
<tr>
<td>X.XX</td>
<td>±0.15</td>
<td>±0.10</td>
</tr>
<tr>
<td>X.XXX.X</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
</tbody>
</table>

### Reference Documents

- FERMI, E.N. #400-1.0s
- This specification takes precedence over documents referenced herein.
- Reference documents shall be given in full on the date of publication for bid.
- Operation beyond the stated voltage or current may result in failure, mechanical stressing or failure.

### Table 1: Dimensions

<table>
<thead>
<tr>
<th>Dimension</th>
<th>MIN</th>
<th>MAX</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
<td>±0.10</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td>±0.10</td>
</tr>
</tbody>
</table>

### Table 2: Performance Ratings

<table>
<thead>
<tr>
<th>Performance Rating</th>
<th>Time to Trip</th>
<th>Resistance Values</th>
<th>Tripped-State Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AMPs</td>
<td>A Hold</td>
<td>MHold</td>
</tr>
<tr>
<td></td>
<td>AMPs</td>
<td>A Hold</td>
<td>MHold</td>
</tr>
</tbody>
</table>

**Notes:**
- All metal surfaces are to be plated.
- Devices cannot be welded or soldered.
- Drawing not to scale.

### Additional Information

- Model No.: PC-9955
- Part No.: PN-0045
- Sheet: 1 of 2
- Scale: 5 mm
- Units: DECIMAL
- Drawn: E4
- Approved: F

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**IOI TECHNOLOGY CORPORATION**

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**Datasheet of non-linear Thermistor**

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**Rev**

**Date**

**Remark**
### Features/Specifications:

- UL 94V-2 nylon 66, Natural color
- Pins: Phosphor bronze Thickness 0.25mm
- Plating tin
- Two P.C tail lengths
- Voltage Rating: 250V AC (R.M.S)
- Current Rating: 6.5 amperes
- Dielectric Withstanding Voltage: 1500 VAC for 60 sec.
- Insulation Resistance: 500 megohms milliohms
- Contact Resistance: 10 milliohms maximum
- Ambient Temperature Range: -40°C to 105°C

### Ordering Information

<table>
<thead>
<tr>
<th>Model No.</th>
<th>P.C Tail Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO-00019</td>
<td>3.6±0.5mm</td>
</tr>
</tbody>
</table>

### Tolerances Unless Noted

<table>
<thead>
<tr>
<th>Feature</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>±0.15</td>
<td>±1°</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.15</td>
</tr>
<tr>
<td>±0.10</td>
<td>±0.10</td>
</tr>
</tbody>
</table>

**NOTE:**

- All dimensions are in mm.
- All tolerances are ±0.05 mm unless otherwise specified.

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**REV**

**DATE**

**REMARK**

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**A**

---

**B**

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**C**

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**D**

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**E**

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**F**

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1 Introduction

1.1 XIO2213B Features

- Full \( \times 1 \) PCI Express™ (PCIe) Throughput
- Fully Compliant With PCI Express Base Specification, Revision 1.1
- Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock
- Fully Compliant With 1394 Open Host Controller Interface (OHCI) Specification, Revision 1.1 and Revision 1.2 Draft
- Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bit/s, 200M Bit/s, 400M Bit/s, and 800M Bit/s
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Cable Power Presence Monitoring
- EEPROM Configuration Support to Load Global Unique ID for 1394 Fabric
- Support for D1, D2, D3_{hot}
- Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link Is Idle, Using Both L0s and L1 States
- Eight 3.3-V Multifunction General-Purpose I/O (GPIO) Terminals
2 Overview

The Texas Instruments XIO2213B is a single-function PCI Express™ (PCIe) to PCI local bus translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b physical layer (PHY). When the XIO2213B is properly configured, this solution provides full PCIe and 1394b functionality and performance.

2.1 Description

The TI XIO2213B is a PCIe to PCI translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b PHY. The PCIe to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Std 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

The XIO2213B simultaneously supports up to four posted write transactions, four nonposted transactions, and four completion transactions pending in each direction at any time. Each posted write data queue and completion data queue can store up to 8K bytes of data. The nonposted data queues can store up to 128 bytes of data.

The PCIe interface supports a ×1 link operating at full 250 Mbit/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the PCI Express Base Specification, Revision 1.1. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency. If parity errors are detected, packet poisoning is supported for both upstream and downstream operations.

PCIe power management (PM) features include active-state link PM, PME mechanisms, and all conventional PCI D states. If the active-state link PM is enabled, the link automatically saves power when idle using the L0s and L1 states. PM active-state NAK, PM PME, and PME-to-ACK messages are supported. The bridge is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption.

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCIe configuration space, allow for further system control and customization.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCIe bus and the 1394 bus at 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s. The device provides three 1394 ports that have separate cable bias (TPBIAS).

As required by the 1394 Open Host Controller Interface (OHCI) Specification, internal control registers are memory mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCIe, and it provides plug-and-play (PnP) compatibility.

The PHY provides the digital and analog transceiver functions needed to implement a 3-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An optional external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.
The XIO2213B requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL. Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbit/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the XIO2213B conforms to IEEE Std 1394b-2002, the BMODE terminal must be asserted. The BMODE terminal does not select the cable-interface mode of operation. BMODE selects the internal PHY-section/LLC-section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation. Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the XIO2213B, this bit can only be set by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.